

LH12232D

■ 特性:

显示内容: 122 x 32 点

驱动方式: 1/32D

可供型号:

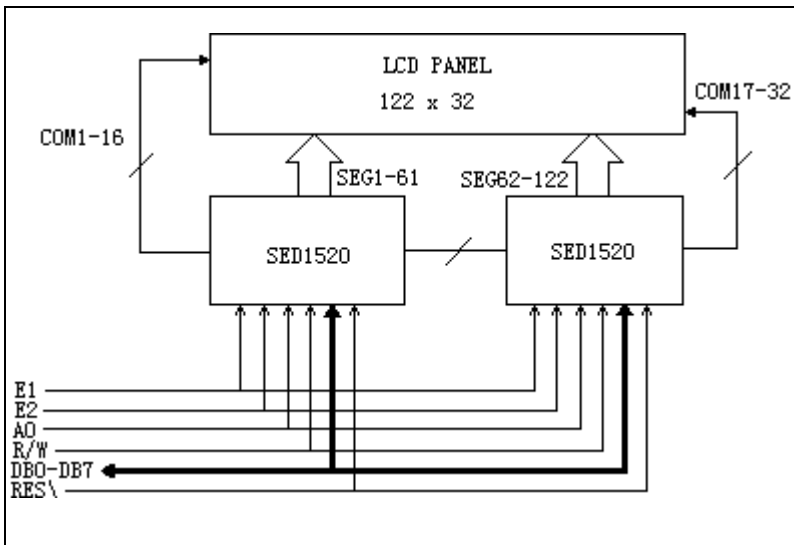
STN(黄绿模、灰模、黑白模)

反射型, 带 EL 或 LED 背光源

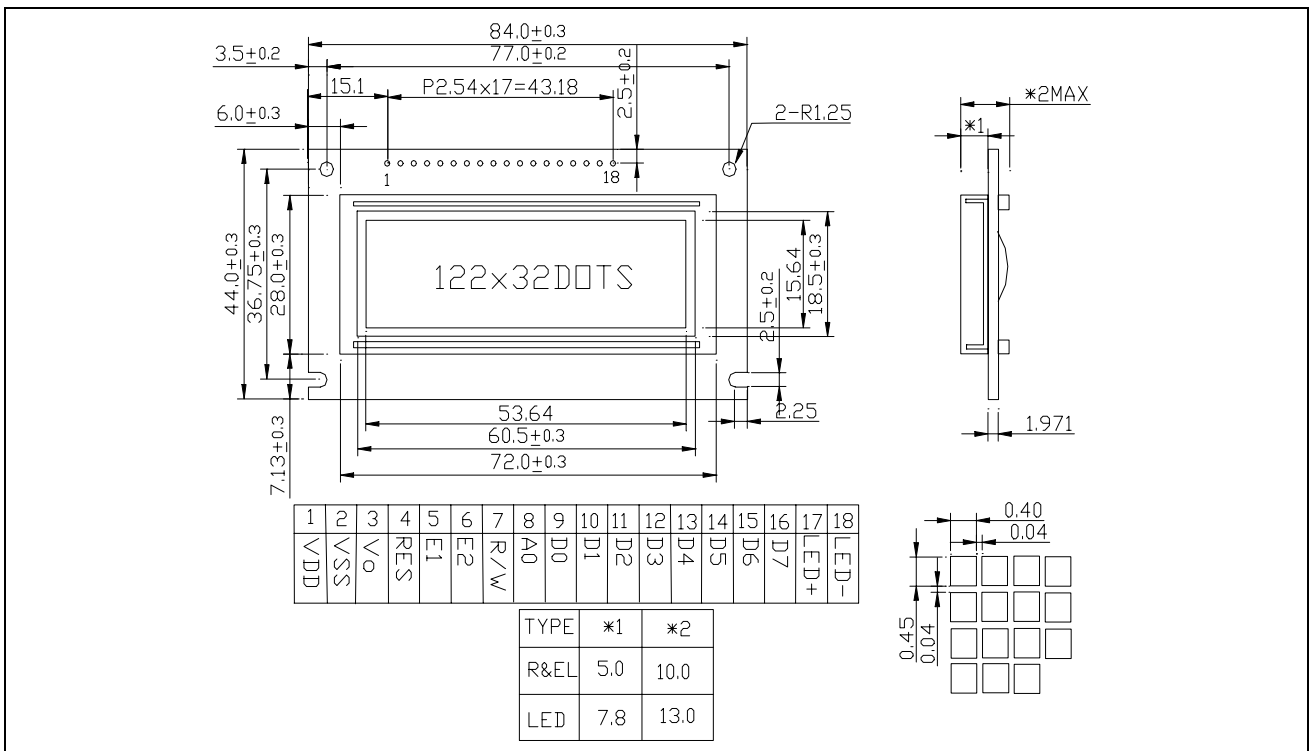
EL/100VAC, 400HZ

LED/4.2VDC

■ 电路图



■ 外形尺寸/显示内容



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■ 极限参数

名称	符号	测试条件	标准值		单位
			最小值	最大值	
电源电压	$V_{DD}-V_{SS}$	$T_a=25^{\circ}\text{C}$	0	6.5	V
LCD 驱动电压	$V_{DD}-V_0$		0	12.0	V
输入电压	V_i		0	V_{DD}	V

■ 电参数

名称		符号	测试条件	标准值			单位
				最小值	典型值	最大值	
电压	逻辑	$V_{DD}-V_{SS}$	-	4.75	5.0	5.25	V
	LCD	$V_{DD}-V_0$	-	4.5	5.5	6.5	V
电流	逻辑	I_{DD}	-	-	2.5	-	mA
	LCD	I_{EE}	-	-	2.0	-	mA
LCD 工作电压 (推荐值)		$V_{DD}-V_0$	0°C	-	6.2	-	V
			25°C	-	5.5	-	V
			40°C	-	4.8	-	V
输入电压	‘H’ 电平	V_{IH}	高电平	$0.7V_{DD}$	-	V_{DD}	V
	‘L’ 电平	V_{IL}	低电平	0	-	$0.3V_{DD}$	V

■ 接口引脚

引脚	符号	电平	说明
1	VDD	5	电源电压
2	VSS	0	(GND)
3	V_0	可调	LCD 驱动电压 (对比度调节)
4	RES	H/L	复位信号
5	E1	H, H→L	片使能信号 1
6	E2	H, H→L	片使能信号 2
7	R/W	H/L	H: 读; L: 写
8	A0	H/L	H: 数据; L: 指令
9	D0	H/L	数据位 0
10	D1	H/L	数据位 1
11	D2	H/L	数据位 2
12	D3	H/L	数据位 3
13	D4	H/L	数据位 4
14	D5	H/L	数据位 5
15	D6	H/L	数据位 6
16	D7	H/L	数据位 7
17	LED+		背光正极
18	LED-		背光负极

AC Characteristics

° Read/Write timing for the 80-port MPU (Ta = -20 to 75°C, VSS = -5.0V±10%)

Parameter	Signal	Symbol	Condition	Rating			Unit	
				Min	Type	Max		
Address hold time	A0, \overline{CS}	t _{AHB}		10	-	-	ns	
Address set-up time		t _{AWB}		20	-	-	ns	
System cycle time	\overline{WR} , \overline{RD}	t _{CYC8}		1000	-	-	ns	
Control pulse width		t _{CC}		200	-	-	ns	
Data set-up time	D0 ~ D7	t _{DS8}		80	-	-	ns	
Data hold time		t _{DH8}		10	-	-	ns	
RD access time		t _{ACC8}	CL = 100pF		-	-	90	ns
Output disable time		t _{OH8}			10	-	60	ns

*. The ratings when VSS = -3.0V are approximately 100% higher than when VSS = -5.0V.

° Read/Write timing for the 68-port MPU (Ta = -20 to 75°C, VSS = -5.0V±10%)

Parameter	Signal	Symbol	Condition	Rating			Unit	
				Min	Type	Max		
System cycle time	A0, \overline{CS} R/W	t _{CYC6} *3		1000	-	-	ns	
Address set-up time		t _{AW6}		20	-	-	ns	
Address hold time		t _{AH6}		10	-	-	ns	
Data set-up time	D0-D7	t _{DS6}		80	-	-	ns	
Data hold time		t _{DH6}		10	-	-	ns	
Output disable time		t _{OH6}	CL = 100pF		10	-	60	ns
Access time		t _{ACC6}			-	-	90	ns
Enable pulse width	READ	E	t _{ew}	100	-	-	ns	
	WRITE			80	-	-	ns	

*. t_{CYC6} indicates the cycle during which CS/E are HIGH; it does not indicate the cycle of the E signal.

*. The ratings when VSS = -3.0V are approximately 100% higher than when VSS = -5.0V.

° Control timing for 80-port/68-port display (Ta = -20 to 75°C, VSS = -5.0V±10%)

Parameter	Signal	Symbol	Condition	Rating			Unit
				Min	Type	Max	
LOW pulse width	CL	t _{WLCL}		35	-	-	μs
HIGH pulse width		t _{WHCL}		35	-	-	μs
Rising time		t _r		-	30	150	ns
Falling time		t _f		-	30	150	ns
FR delay time	FR	t _{DFR}	(Input timing)	-2.0	0.2	2.0	μs
			(Output timing), CL = 100pF	-	0.2	0.4	

*. The ratings when VSS = -3.0V are approximately 100% higher than when VSS = -5.0V.

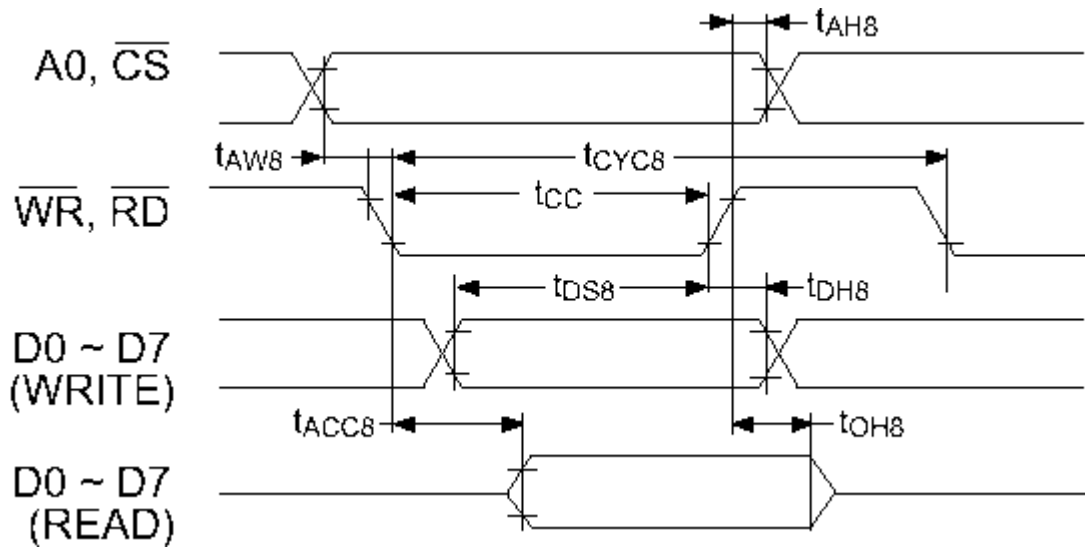
*. The input timing of the FR delay time is determined by the SED1520 (Slave).

The output timing of the FR delay time is determined by the SED1520 (Master).

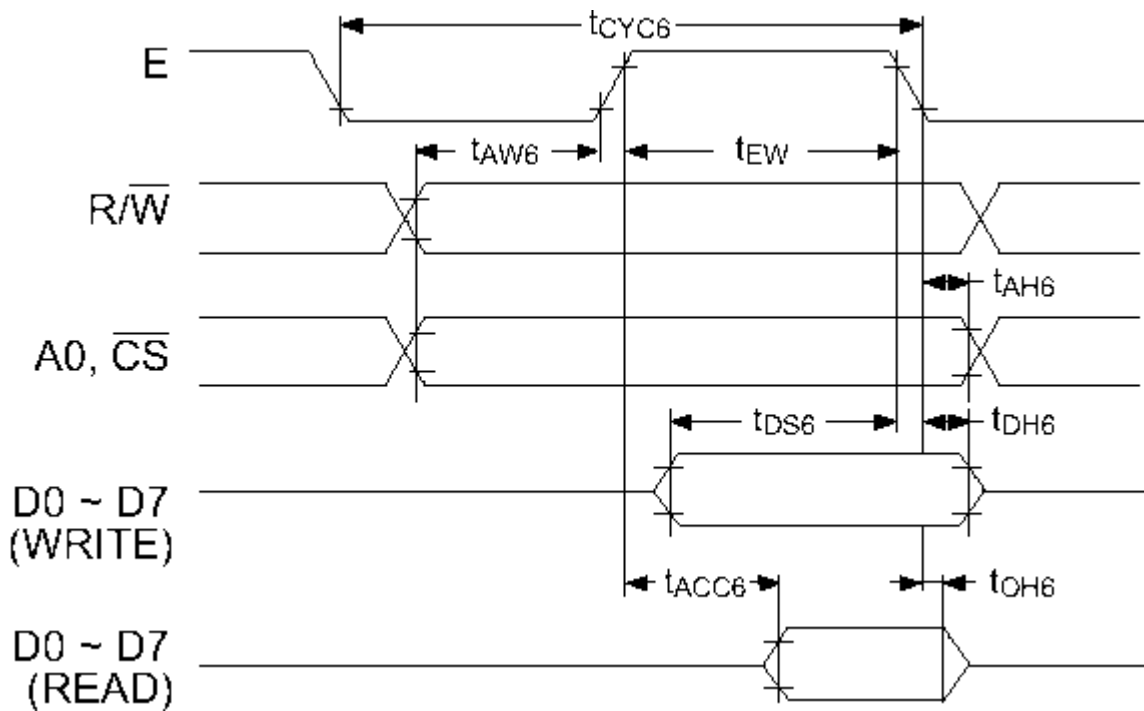
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• Timing Chart

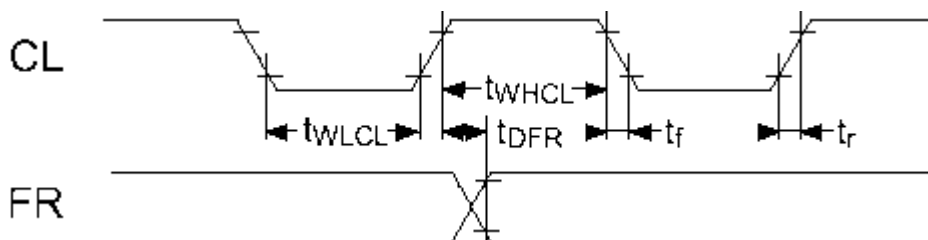
◦ Read/Write timing for the 80-port MPU



◦ Read/Write timing for the 68-port MPU



◦ Control timing for 80-port/68-port display



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■ MODEL CLASSIFICATION

Model Name	Operating Clock		Connectable Drivers	SEG Driver	COM driver
	Internal oscillator	External clock			
SED1520Fo*	18 KHz	18 kHz	SED1520Fo*, SED1521Fo*	61 ports	16 ports
SED1520FA*	-	2 KHz	SED1520FA*, SED1521FA*	61 ports	16 ports

■ DISPLAY COMMANDS

(Based on the 80-port MPU; the RD and WR commands differ for the 68-port MPU.)

Command		RD WR A0	D7 D6 D5 D4 D3 D2 D1 D0	Function
1	Display ON/OFF	1 0 0	1 0 1 0 1 1 1 0/1	Switches the entire display ON or OFF, regardless of the Display RAM's data or the internal status. **
2	Display START Line	1 0 0	1 1 0 Display START address (0~31)	Determines the line of RAM data to be displayed at the display's top line (COM0).
3	Page Address Set	1 0 0	1 0 1 1 1 0 Page (0~3)	Sets the page of the Display RAM in the page address register.
4	Column (Segment) Address Set	1 0 0	0 Column address (0~79)	Sets the column address of the Display RAM in the column address register.
5	Status Read	0 1 0	BUSY ACC ON/OFF RESET 0 0 0 0	Reads the status. BUSY 1: Busy (internal processing) 0: READY status ADC 1: Rightward (forward) output 0: Leftward (reverse) output ON/OFF 1: Display OFF 0: Display ON RESET 1: Resetting 0: Normal
6	Write Display Data	1 0 1	Write Data	Writes the data on the data bus to RAM
7	Read Display Data	0 1 1	Read Data	Reads data from the Display RAM onto the data bus.
8	ADC Select	1 0 0	1 0 1 0 0 0 0 0/1	Used to reverse the correspondence between the Display RAM's column addresses and segment driver output ports 0: Rightward (forward) output 1: Leftward (reverse) output
9	Static Drive ON/OFF	1 0 0	1 0 1 0 0 1 0 0/1	Selects normal display operation or static all-lit drive display operation. 1: Static drive (Power Save) **; 0: Normal display operation
10	Duty Select	1 0 0	1 0 1 0 1 0 0 0/1	Selects the duty factor for driving LCD cells. 1: 1/32 duty 0: 1/16 duty
11	Read Modify Write	1 0 0	1 1 1 0 0 0 0 0	Increments the column address counter by one only when display data is written but not when it is read.
12	End	1 0 0	1 1 1 0 1 1 1 0	Cancels the Ready Modify Write mode.
13	Reset	1 0 0	1 1 1 0 0 0 1 0	Resets the Display START line to the 1st line in the register. Resets the column address counter to 0 and page address register to 3.

** . Power Save mode is entered by selecting static drive in Display OFF status.